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For:	PROTECTION CIRCUIT FOR MOS COMPONENTS (As Amended)		

LETTER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

August 17, 2004

Sir:

Further to our March 30, 2004 Letter submitting a Certified English translation of Taiwanese priority document No. 090105923, filed on March 14, 2001, we are attaching a revised English translation of Taiwanese priority document No. 090105923.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fee required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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Attachment

TITLE

Method for protecting MOS components from antenna effect and the apparatus thereof

ABSTRACT OF THE DISCLOSURE

A method for protecting MOS components from antenna effect and the apparatus thereof. Via the bypass PMOS and NMOS transistors, charges with either polarity accumulated by antenna effect are conveyed and neutralized. The present invention thus protects the gate oxide layer of the MOS component in the IC circuit from damage or degradation.

ILLUSTRATION OF THE INVENTION

The present invention relates in general to a method to protect MOS components and the apparatus thereof, and more particular, to a method to protect MOS components from antenna effect and the apparatus thereof.

During plasma etching, damaging induced by plasma to the MOS component is referred to as plasma charging damaging, or antenna effect. Due to the uneven distribution characteristics of charges in plasma, charges are accumulated on the conductors (such as: polysilicon or aluminum alloys) with large surface areas or long sides. The charges generate an electric field on the gate oxide layer of the MOS component. When enough charges are collected, the electric field across the gate oxide layer changes the properties of the MOS component. More severe damage may occur if the current is high enough to pass through the gate oxide layer.

Fig.1 shows a conventional circuit design using a diode to reduce the antenna affect. In Fig.1, T1 is a MOS component in an integrated circuit (IC), the substrate (or bulk) B of the MOS is coupled to its own source, or to a positive power rail VDD (or a negative power rail VSS). The diode D1 has its anode coupled to the substrate of the IC. It is assumed that the conductive line L1 connected with the gate of the MOS component T1 has a very large surface area or periphery length. Due to the plasma characteristics, a large amount of charges is accumulated on the conductive line L1, causing the antenna affect (as the antenna shown in Fig.1).

If the accumulated charges are negative charges, the diode D1 provides a discharge path to release the negative charges to the substrate of the IC, preventing damaging made to the gate

oxide layer of the MOS component T1. However, when the accumulated charges are positive charges, no discharge path exists. The electric field across the gate oxide layer thus degrades the layer. Moreover, the large stray capacitance of the diode D1 compromises the operating rate of the IC circuit, resulting in slower operating speeds.

Fig.2 shows a conventional circuit design using a transmission gate to reduce the antenna effect. In Fig.2, the conductive line L2 connected to the gate of the MOS component T2 has very a large area or is very long. Due to the plasma distribution characteristics, large amounts of charges are accumulated on the conductive line L2, causing the antenna effect (as the antenna shown in Fig.2). Herein, T2 is the MOS component of a IC circuit with its substrate B connected to the source or a positive power rail VDD (or a negative power rail VSS).

To reduce the antenna effect, a transmission gate is placed in the IC circuit in Fig.2 and coupled with the gate of the MOS component T2. In the NMOS transistor NT of the transmission gate, the gate and the substrate are respectively coupled to the nodes VDD and VSS. In the PMOS transistor PT of the transmission gate, the gate and the substrate are respectively coupled to the nodes VSS and VDD. Irrespective of whether the accumulated charges in the antenna effect are of either of the bias polarities, they are discharged through the parasitic diodes between the source/drain and the substrate of the NMOS transistor NT (or PMOS transistor PT) to prevent the MOS component T2 from degradation.

Because the transmission gate is located on the path for controlling the gate of the MOS component T2, and the

transmission gate has parasitic capacitor C and resistance R, the RC constant will lead to the delay of the control signal sent to the gate of T2 and compromise the operating rate of the MOS component T2. To enhance the operating rate of the MOS component T2, resistance R is expected to be reduced. The easiest way to reduce the resistance R is to cut the channel length or increase the channel width of the transmission gate. However, by doing so, the capacitance C is simultaneously increased. Therefore, it is awkward to reduce the antenna effect by adjusting the R and C values according to the configuration in Fig.2.

In view of this, an object of the present invention is to provide a method for protecting an MOS component from the antenna effect and the apparatus thereof. In the present invention, via the bypass PMOS and NMOS transistors, charges with either polarity accumulated by antenna effect are conveyed and neutralized, thereby protecting the gate oxide layer of the MOS component in the IC circuit from damage or degradation

According to the above object, the present invention provides a method for protecting an MOS component from antenna effect. The method comprises disposal, between a first voltage node and the MOS component, of a bypass PMOS transistor, the gate, source and substrate of which are coupled to the first voltage node and the drain of which is coupled to the gate of the MOS component; and disposal, between a second voltage node and the MOS component, of a second bypass NMOS transistor, the gate, source and substrate of which are coupled to the second voltage node and the drain of which is coupled to the gate of the MOS component.

When positive charges accumulate on the gate of the MOS component due to the antenna effect, the bypass PMOS transistor

conveys the positive charges to the first voltage node to prevent them from entering and damaging the MOS component. When the negative charges accumulate on the gate of the MOS component due to the antenna effect, the bypass NMOS transistor conveys the negative charges to the second voltage node to prevent them from entering and damaging the MOS component.

According to the above object, the present invention provides an apparatus for protecting an MOS component from antenna effect. The apparatus includes a bypass PMOS transistor whose gate, source and substrate are coupled to a first voltage node, wherein the bypass PMOS transistor conveys the positive charges to the first voltage node to prevent them from entering and damaging the MOS component when positive charges are accumulated on the gate of the MOS component due to antenna effect; and a bypass NMOS transistor, whose gate, source and substrate are coupled to a second voltage node, wherein the bypass NMOS transistor conveys the negative charges to the second voltage node to prevent them from entering and damaging the MOS component when negative charges are accumulated on the gate of the MOS component due to the antenna effect.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be more fully understood by reading the subsequent detailed description in conjunction with the examples and references made to the accompanying drawings, wherein:

Fig. 1 is a perspective diagram of a conventional circuit using a diode to reduce the antenna effect;

Fig. 2 is a perspective diagram of a conventional circuit using a transmission gate to reduce the antenna effect; and

Fig. 3 shows the embodiment of the present invention for reducing the antenna effect.

DESCRIPTION OF SYMBOL

D1~diode;

T1-T3~NMOS transistor;

Antenna~antenna effect;

T~NMOS transistor;

PT~PMOS transistor;

L1-L3~conductive line;

BN~bypass NMOS transistor;

BP~bypass NMOS transistor;

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Fig.3 shows a circuit of the embodiment of the present invention to reduce the antenna effect.

Referring to Fig.3, the present invention provides a method for protecting a MOS component from antenna effect. The method comprises:

(1) The disposal, between a first voltage node VDD and the MOS component T3, of a bypass PMOS transistor BP, the gate, source and substrate of which are coupled to the first voltage node VDD and the drain of which is coupled to the gate of the MOS component T3 through conductive line L3; and

(2) Disposal, between a second voltage node VSS and the MOS component T3, of a bypass NMOS transistor BN, the gate, source and substrate of which are coupled to the second voltage node VSS, and the drain of which is coupled to the gate of the MOS component T3 through conductive line L3.

In this embodiment, the MOS transistor T3 is a NMOS transistor, but it also can be a PMOS transistor.

Referring to Fig.3, according to the method described, the following apparatus is proposed for protecting an MOS component from the antenna effect, the apparatus comprising:

(1) a bypass PMOS transistor BP, the gate, source and the substrate of which are coupled to a first voltage node VDD, and the stray diode of which, when positive charges are accumulated on the gate of the MOS component through the conductive line L3 due to the antenna effect, conveys the positive charges to the first voltage node VDD to prevent the positive charges from entering and damaging the gate oxide layer of the MOS component T3; and

(2) a bypass NMOS transistor BN, the gate, source and substrate of which are coupled to a second voltage node VSS, and the stray diode of which, when the negative charges are accumulated on the gate of the MOS component T3 through the conductive line L3 due to the antenna effect, conveys the negative charges to the second voltage node VSS to prevent them from entering and damaging the gate oxide layer of the MOS component T3.

Therefore, the present invention has the following advantages:

(1) Conveyance of the positive charges accumulated through the antenna effect to the voltage node VDD via the bypass PMOS transistor BP; and of the negative charges accumulated through the antenna effect to the voltage node VSS via the bypass NMOS transistor NP. Thus, the present invention neutralizes the accumulated charges of either polarity.

(2) The present invention uses bypass NMOS and PMOS transistors, wherein the stray capacitances are between the drains and substrates of the bypass transistors only. Compared to the transmission gate in Fig.2, the design of the present invention reduces the parasitic capacitance substantially, and the resistance referred in Fig.2 is omitted. Thus the operating rate of the protected component is enhanced.

(3) The bypass NMOS and PMOS transistors in the present invention enhance the compatibility of IC circuit with MOS process with other MOS component.

Finally, while the invention has been described by way of example and in terms of the preferred embodiment, it is to be understood that the invention is not limited to the disclosed embodiments. On the contrary, it is intended to cover various modifications and similar arrangements as would be apparent to those skilled in the art. Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

What Is Claimed Is:

1. An apparatus for protecting a MOS component from antenna effect, the apparatus comprising:

a bypass PMOS transistor, having a gate, a source and a substrate, all coupled to a first voltage node; wherein when positive charges are accumulated on the gate of the MOS component due to antenna effect, the bypass PMOS transistor conveys the positive charges to the first voltage node to prevent the positive charges from entering and damaging the MOS component; and

a bypass NMOS transistor, having a gate, a source and a substrate, all coupled to a second voltage node; when negative charges are accumulated on the gate of the MOS component due to antenna effect, the bypass NMOS transistor conveys the negative charges to the second voltage node to prevent the negative charges from entering and damaging the MOS component.

2. A method for protecting a MOS component from antenna effect, comprising:

Disposal, between a first voltage node and the MOS component, of a bypass PMOS transistor the gate, the source and substrate of which are coupled to the first voltage node and the drain of which is coupled to the gate of the MOS component; and

Disposal, between a second voltage node and the MOS component, of a bypass NMOS transistor the gate, source and substrate of which are coupled to the

second voltage node and the drain of which is coupled to the gate of the MOS component;

wherein when positive charges are accumulated on the gate of the MOS component due to antenna effect, the bypass PMOS transistor conveys the positive charges to the first voltage node to prevent the positive charges from entering and damaging the MOS component; when negative charges are accumulated on the gate of the MOS component due to antenna effect, the bypass NMOS transistor conveys the negative charges to the second voltage node to prevent the negative charges from entering and damaging the MOS component.

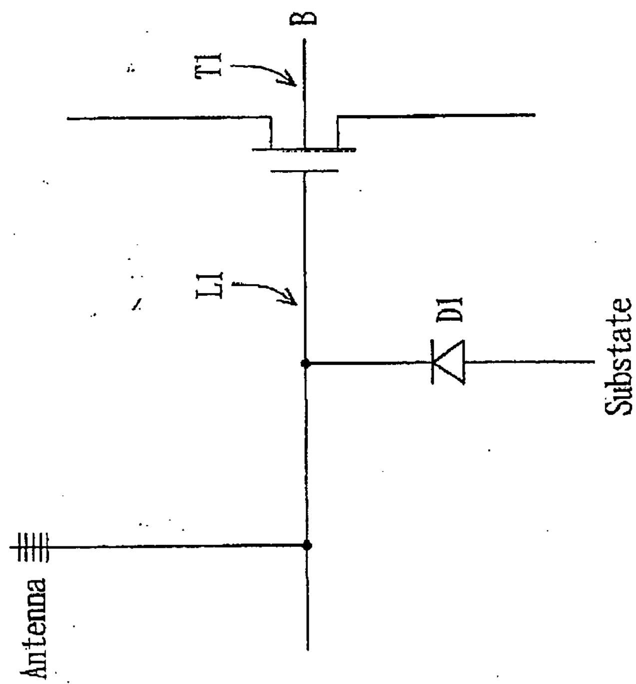

FIG. 1

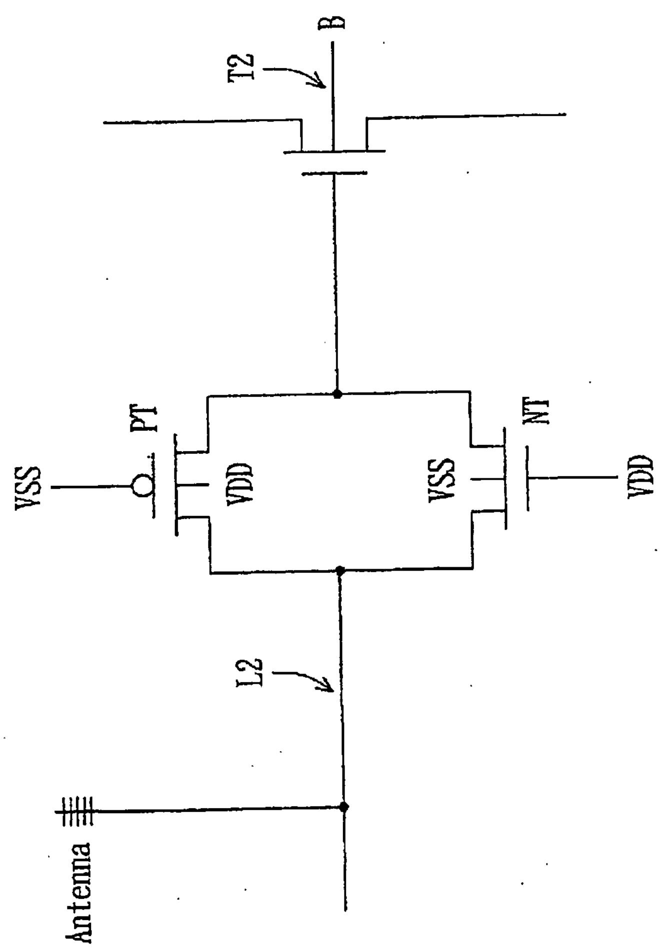

FIG. 2

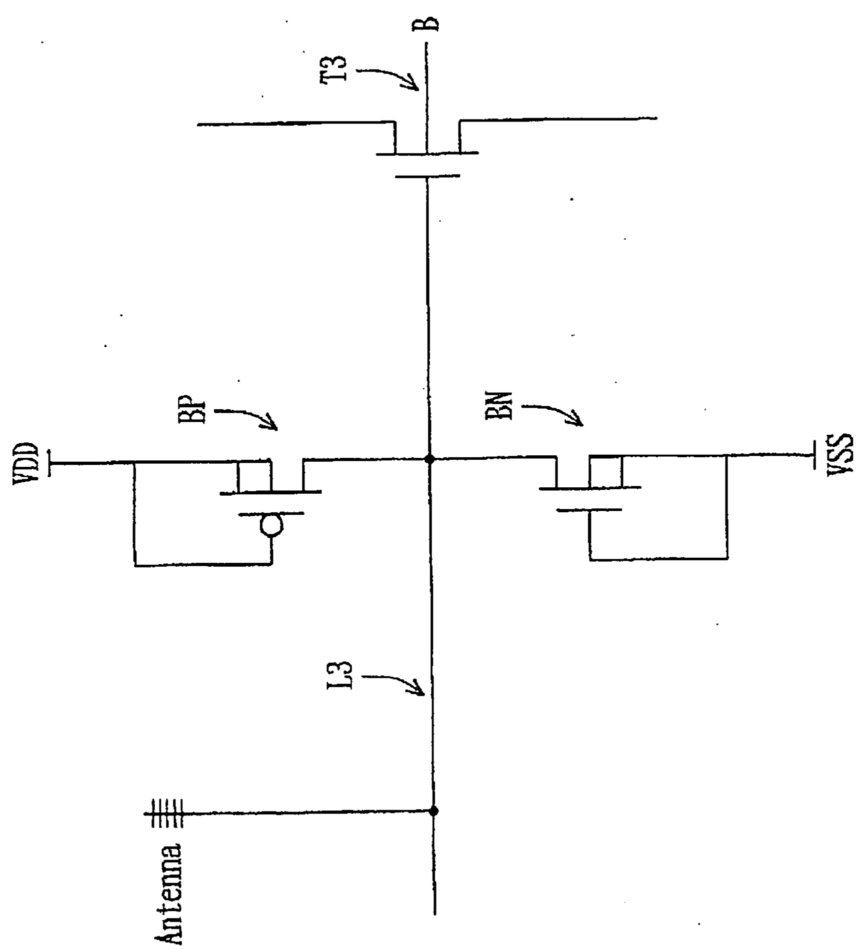

FIG. 3